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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,321	02/27/2004	Kevin Faulkner	6502.0570	4320

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EXAMINER	
MEHRMANESH, ELMIRA	

ART UNIT	PAPER NUMBER
2113	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/787,321	FAULKNER ET AL.	
	Examiner	Art Unit	
	Elmira Mehrmanesh	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The application of FAULKNER et al., for a "SYSTEMS AND METHODS FOR PERFORMING QUIESCENCE IN A STORAGE VIRTUALIZATION ENVIRONMENT" filed February 27, 2004 has been examined.

Claims 1-25 are presented for examination.

Information disclosed and listed on PTO 1449 has been considered.

Claims 20-25 are rejected under 35 USC § 101.

Claims 14-25 are rejected under 35 USC § 102.

Claims 1-13 are rejected under 35 USC § 103.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 20-25 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

In view of Applicant's disclosure, specification [0175], page 81, the medium is not limited to tangible embodiments, instead being defined as including both tangible embodiments (e.g., specification [0175], page 81, floppy disk, CD, DVD) and intangible embodiments (e.g., specification [0175], page 81, via network which implies the use of intangible media such as signals, carrier waves). As such, the claim is not limited to statutory subject matter and is therefore non-statutory.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marks et al. (U.S. Patent No. 5,790,775) in view of Bishop et al. (U.S. Patent No. 5,539,875).

As per claim 1, Marks discloses a method comprising:

configuring a virtualization layer (Fig. 3) to interface between a host (Fig. 3, element 12) and at least one storage device (Fig. 3, element 40), wherein the virtualization layer defines at least one virtual volume comprising objects defining a mapping to data in the at least one storage device (Fig. 3)

storing information about a state of the at least one storage device in a virtualization database that is distributed across more than one processor in a the virtualization layer (Fig. 4, element 56)

establishing a state manager for each of the more than one processors, wherein the state manager monitors the state of the at least one storage device (col. 8, lines 42-50)

Marks fails to explicitly disclose a quiescence instruction.

Bishop et al. teaches:

issuing a quiescence instruction to the state manager for each of the more than one processors, and responsive to receiving a quiescence instruction by the state manager, completing shod term operations underway at the time the quiescence instruction is received, and halting long term operations underway at the time the quiescence instruction is received (col. 10, lines 10-43).

It would have been obvious to one of ordinary skill in the art at the time the invention to use the method of storage controller failover/failback of storage devices of Marks et al.'s in combination with the storage subsystem recovery of Bishop et al.

One of ordinary skill in the art at the time the invention would have been motivated to make the combination because Marks et al. discloses a fault tolerant system having storage controller failover and failback support for increased data availability (col. 2, lines 65-68). Bishop et al. discloses a method of error detection and recovery among storage devices (col. 2, lines 44-49).

As per claim 2, Marks fails to explicitly disclose a quiescence instruction.

Bishop et al. teaches:

issuing the quiescence instruction when a storage device fails (col. 10, lines 10-14).

As per claim 3, Marks fails to explicitly disclose a quiescence instruction.

Bishop et al. teaches:

issuing the quiescence instruction when a processor fails (Fig. 2).

As per claim 4, Marks fails to explicitly disclose a quiescence instruction.

Bishop et al. teaches:

receiving notification from the state managers when short term operations are completed and long term operations are halted (Fig. 5, element 142).

As per claim 5, Marks fails to explicitly disclose a quiescence instruction.

Bishop et al. teaches:

the short term operations include at least one of: a read operation and a write operation (Figs. 7A-7F).

As per claim 6, Marks discloses the long term operations include at least one of: rebuilding a virtual volume and scrubbing a virtual volume (col. 7, lines 14-18) and (Fig. 7A, element 106).

As per claim 7, Marks discloses reconfiguring the virtualization layer after the notification has been received from the state managers (col. 7, lines 14-18).

As per claim 8, Marks discloses the configuring layer does not interface with a device that has failed (col. 7, lines 14-18).

As per claim 9, Marks discloses a system comprising:

a plurality of storage devices (Fig. 3, element 40) storing data corresponding to a host (Fig. 3, element 12)

a virtualization layer between the host and the plurality of storage devices (Fig. 3, element 40), the virtualization layer comprising objects defining a mapping to data in the plurality of storage devices (Fig. 3)

a virtualization database storing information about a state of each of the plurality of storage devices (Fig. 4, element 56)

a plurality of processor, each processor having a state manager that monitors the state of at least one storage device corresponding to the processor (col. 8, lines 42-50)

Marks fails to explicitly disclose a quiescence instruction.

Bishop et al. teaches:

receives a quiescence instruction in response to a change in the state of one of the plurality of storage devices, and, responsive to receiving the quiescence instruction, completes short term operations underway at the time the quiescence instruction is

received and halts long term operations underway at the time the quiescence instruction is received (col. 10, lines 10-43).

As per claim 10, Marks fails to explicitly disclose a quiescence instruction.

Bishop et al. teaches:

a master one of the plurality of processors that issues the quiescence instruction in response to a failure of one of the plurality of storage devices (col. 12, lines 11-18).

As per claim 11, Marks fails to explicitly disclose a quiescence instruction.

Bishop et al. teaches:

each processor's state manager further notifies the master processor when short term operations are complete and long term operations are halted (Fig. 5, element 142).

As per claim 12, Marks discloses the master processor further reconfigures the virtualization layer after notification is received from each processor's state manager that short term operations are complete and long term operations are halted (col. 7, lines 14-18).

As per claim 13, Marks discloses the virtualization database is distributed across more than one processor in the virtualization layer (Fig. 4).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 14-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Marks et al. (U.S. Patent No. 5,790,775).

As per claim 14, Marks discloses a system for dynamically updating storage associated with a host (col. 8, lines 42-50) and (col. 7, lines 14-18) comprising:

means for configuring a virtualization layer (Fig. 3) to interface between a host (Fig. 3, element 12) and at least one storage device (Fig. 3, element 40), wherein the virtualization layer defines at least one virtual volume comprising objects defining a mapping to data in the at least one storage device (Fig. 3)

means for storing information about a state of a storage device corresponding to the host in a virtualization database means for receiving data about a new state of the storage device corresponding to the host (Fig. 4, element 56)

means for updating the virtualization database with the data about the new state of the storage device (col. 8, lines 42-50) and (col. 7, lines 14-18)

means for updating the mapping contained in the objects comprising the virtual volume based on the data about the new state of the storage device (col. 8, lines 42-50) and (col. 7, lines 14-18).

As per claim 15, Marks discloses the virtualization database is distributed across more than one processor in the virtualization layer (Fig. 3).

As per claim 16, Marks discloses the new state of the storage device is responsive to the storage device becoming available (col. 8, lines 42-50) and (col. 7, lines 14-18).

As per claim 17, Marks discloses the new state of the storage device is responsive to the storage device becoming unavailable (col. 8, lines 42-50) and (col. 7, lines 14-18).

As per claim 18, Marks discloses means for reconfiguring the virtualization layer after the mapping has been updated, wherein the reconfigured virtualization layer does not interface with the unavailable storage device (col. 7, lines 14-18).

As per claim 19, Marks discloses means for reconfiguring the virtualization layer after the mapping has been updated, wherein the reconfigured virtualization layer interfaces with the available storage device (col. 7, lines 14-18).

As per claim 20, Marks discloses a computer-readable medium (Fig. 4, element 46), containing code (Fig. 4, element 54) for directing a processor to perform a method

for dynamically updating storage associated with a host (col. 8, lines 42-50) and (col. 7, lines 14-18), the method comprising:

configuring a virtualization layer (Fig. 3) to interface between a host (Fig. 3, element 12) and at least one storage device (Fig. 3, element 40), wherein the virtualization layer defines at least one virtual volume comprising objects defining a mapping to data in the at least one storage device (Fig. 3)

storing information about a state of a storage device corresponding to the host in a virtualization database (Fig. 4, element 56)

receiving data about a new state of the storage device corresponding to the host updating the virtualization database with the data about the new state of the storage device (col. 8, lines 42-50) and (col. 7, lines 14-18)

updating the mapping contained in the objects comprising the virtual volume based on the data about the new state of the storage device (col. 8, lines 42-50) and (col. 7, lines 14-18).

As per claim 21, Marks discloses the virtualization database is distributed across more than one processor in the virtualization layer (Fig. 4).

As per claim 22, Marks discloses the new state of the storage device is responsive to the storage device becoming available (col. 8, lines 42-50) and (col. 7, lines 14-18).

As per claim 23, Marks discloses the new state of the storage device is responsive to the storage device becoming unavailable (col. 8, lines 42-50) and (col. 7, lines 14-18).

As per claim 24, Marks discloses reconfiguring the virtualization layer after the mapping has been updated, wherein the reconfigured virtualization layer interfaces with the unavailable storage device (col. 7, lines 14-18).

As per claim 25, Marks discloses reconfiguring the virtualization layer after the mapping has been updated, wherein the reconfigured virtualization layer interfaces with the available storage device (col. 7, lines 14-18).

Related Prior Art

The following prior art is considered to be pertinent to applicant's invention, but nor relied upon for claim analysis conducted above.

Schmuck (U.S. Patent No. 6,622,259), "Non-disruptive migration of coordinator services in a distributed computer system".

Harper (U.S. Patent No. 6,675,316), "Method and system for recovery of the state of a failed CPU/cache/memory node in a distributed shared memory system".

Andrewartha (U.S. Patent No. 5,754,557), "Method for refreshing a memory, controlled by a memory controller in a computer system, in a self-refresh mode while scanning the memory controller".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elmira Mehrmanesh whose telephone number is (571) 272-5531. The examiner can normally be reached on 8-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).